WHAT IS CLAIMED IS:

1. A data communication method including:

receiving an *n*-bit block of binary data;

encoding or decoding between the *n*-bit block of binary data and a representation of an *m*-symbol code word, each of the *m*-symbols in the code word including at least five possible values, each code word including:

at least one pair of adjacent symbols including a predetermined type of transition between different values of the symbols of the pair; and

a word disparity representing an cumulative deviation from a baseline of the values of the symbols of the code word, the word disparity being bounded within a predetermined range.

2. The method of claim **1**, in which the encoding or decoding comprises each code word further including an intraword disparity representing a symbol-by-symbol cumulative deviation from baseline, within the code word, the intraword disparity bounded within a predetermined range.

3. The method of claim **2**, in which the coding or decoding comprises:

each code word with a zero word disparity further including an intraword disparity bounded within a first predetermined range;

each code word with a positive word disparity further including an intraword disparity bounded within a second predetermined range;

each code word with a negative word disparity further including an intraword disparity bounded within a third predetermined range; and

in which each of the first, second, and third predetermined ranges includes at least one bound that is different from at least one bound of the others of the first, second, and third predetermined ranges.

4. The method of claim **3**, in which, if the five possible values are represented as (-1, -1/2, 0, +1/2, +1),

the first predetermined range is between -1.5 and +1.5, inclusive;

the second predetermined range is between -1.5 and +3.5, inclusive; and

the third predetermined range is between -3.5 and +1.5, inclusive.

5. The method of claim **1**, in which the predetermined range bounding the word disparity is between -2 and +2, inclusive.

6. The method of claim **1**, in which the encoding or decoding includes encoding or decoding between a 12-bit block of binary data and a representation of a 6-symbol code word.

7. The method of claim **1**, in which the encoding or decoding includes encoding or decoding between the *n*-bit block of binary data and a binary-encoded representation of the *m*-symbol code word.

8. The method of claim **1**, in which the encoding or decoding includes an *m*-symbol code word in which the predetermined type of transition includes a symmetric about baseline transition.

9. The method of claim **8**, in which the symmetric about baseline transition includes a symmetric about zero transition.

10. The method of claim **1**, in which the encoding or decoding includes the five possible values represented as -1, -1/2, 0, +1/2, and +1.

11. The method of claim **10**, in which the five possible values represented as -1,

-1/2, 0, +1/2, and +1 respectively correspond to signal levels of about -100 mV, about -50 mV, about 0 V, about +50 mV, and about +100 mV.

12. The method of claim **1**, further including communicating the *m*-symbol code word using pulse amplitude modulation.

13. The method of claim **1**, in which the encoding or decoding comprises each *m*-symbol code word including:

a first bounded run length of the number of consecutive symbols, from the start of the code word, that do not include a transition of the predetermined type between adjacent ones of the symbols; and

a second bounded run length of the number of consecutive symbols, from the end of the code word, that do not include a transition of the predetermined type between adjacent ones of the symbols.

14. The method of claim **13**, in which the encoding or decoding comprises each *m*-symbol code word includes at least one of:

a first bounded run length of at least six symbols and a second bounded run length of at least five symbols; and

a first bounded run length of at least five symbols and a second bounded run length of at least six symbols.

15. The method of claim **1**, further including pairing *m*-symbol code words with an amount of positive word disparity with corresponding code words with the same amount of negative word disparity, each code word pair mapping to a unique code of the *n*-bit block of binary data, and each code word with zero word disparity mapping to a unique code of the *n*-bit block of binary data.

16. The method of claim **1**, in which the pairing includes pairing code words with an amount of positive word disparity with corresponding symmetric code words with the same amount of negative word disparity.

15. The method of claim **1**, further including using an *m*-symbol nondata code word.

16. The method of claim **15**, in which the *m*-symbol nondata code word is distinct from all *m*-symbol strings of consecutive symbols in all combinations of concatenated pairs of other *m*-symbol code words.

17. The method of claim **15**, in which the nondata code word is distinguishable from all other code words even if a transmission error occurs in one symbol of the nondata code word.

18. The method of claim **1**, in which the encoding or decoding comprises each *m*-symbol code word used for communicating data selected to generally reduce susceptibility to a single-symbol error during communication.

19. The method of claim **1**, further including communicating the *m*-symbol code word.

20. The method of claim **19**, further including:

computing a running disparity, the running disparity representing a cumulative deviation from baseline over a period of interest; and

determining whether to invert the *m*-symbol code word, for the communicating, using the running disparity and the word disparity of the code word.

21. The method of claim **19**, in which the determining whether to invert the *m*-symbol code word includes:

inverting the code word if the running disparity and word disparity are both postive; and

inverting the code word if the running disparity and word disparity are both negative.

22. The method of claim **21**, in which the determining whether to invert the *m*-symbol code word further includes determining to not invert the code word otherwise.

23. The method of claim **19**, further including error checking a received *m*-symbol code word using the running disparity and the word disparity.

24. The method of claim **19**, further including communicating an *m*-symbol nondata code word for aligning word boundaries of received *m*-symbol code words to word boundaries of transmitted *m*-symbol code words.

25. A data communication apparatus including an encoder, the encoder including a map circuit, the map circuit including a first input configured to receive an *n*-bit block of binary data, and a first output configured to provide a representation of at least one corresponding *m*-symbol code word stored in the map, each of the *m*-symbols in the code word including at least five possible values, each code word including:

at least one pair of adjacent symbols including a predetermined type of transition between different values of the symbols of the pair; and

a word disparity representing an cumulative deviation from a baseline of the values of the symbols of the code word, the word disparity being

bounded within a predetermined range, the word disparity stored in the map corresponding to the code word.

26. The apparatus of claim **25**, in which each stored *m*-symbol code word includes an intraword disparity, representing a symbol-by-symbol cumulative deviation from baseline, within the code word, in which the intraword disparity bounded within a predetermined range.

27. The apparatus of claim **26**, in which:

each code word with a zero word disparity further includes an intraword disparity bounded within a first predetermined range;

each code word with a positive word disparity further includes an intraword disparity bounded within a second predetermined range;

each code word with a negative word disparity further includes an intraword disparity bounded within a third predetermined range; and

in which each of the first, second, and third predetermined ranges includes at least one bound that is different from at least one bound of the others of the first, second, and third predetermined ranges.

28. The apparatus of claim **27**, in which, if the five possible values are represented as (-1, -1/2, 0, +1/2, +1),

the first predetermined range is between -1.5 and +1.5, inclusive;

the second predetermined range is between -1.5 and +3.5, inclusive; and

the third predetermined range is between -3.5 and +1.5, inclusive.

29. The apparatus of claim **25**, in which each stored *m*-symbol code word includes a word disparity bounded in a predetermined range between -2 and +2, inclusive.

30. The apparatus of claim **29**, in which each stored *m*-symbol code word includes a word disparity bounded in a predetermined range between 0 and +2, and each stored *m*-symbol code word having positive word disparity also represents a corresponding symmetric *m*-symbol code word having negative word disparity.

31. The apparatus of claim **29**, in which each stored *m*-symbol code word includes a word disparity bounded in a predetermined range between 0 and -2, and each stored *m*-symbol code word having negative word disparity also represents a corresponding *m*-symbol code word having positive word disparity.

32. The apparatus of claim **25**, in which the first input of the map circuit is an addressing input configured to map a particular code of a 12-bit block of binary data to a binary-encoded representation of a 6-symbol code word stored in the map.

33. The apparatus of claim **25**, in which the predetermined type of transition of the *m*-symbol code word includes a symmetric about baseline transition.

34. The apparatus of claim **33**, in which the symmetric about baseline transition includes a symmetric about zero transition.

35. The apparatus of claim **25**, in which each *m*-symbol code word stored in the map includes:

a first bounded run length of the number of consecutive symbols, from the start of the code word, that do not include a transition of the predetermined type between adjacent ones of the symbols; and

a second bounded run length of the number of consecutive symbols, from the end of the code word, that do not include a transition of the predetermined type between adjacent ones of the symbols.

36. The apparatus of claim **35**, in which each *m*-symbol code word stored in the map includes at least one of:

a first bounded run length of at least six symbols and a second bounded run length of at least five symbols; and

a first bounded run length of at least five symbols and a second bounded run length of at least six symbols.

37. The apparatus of claim **25**, in which the map pairs *m*-symbol code words with an amount of positive word disparity with corresponding code words with the same amount of negative word disparity, each code word pair mapping to a unique code of the *n*-bit block of binary data, and each code word with zero word disparity mapping to a unique code of the *n*-bit block of binary data, and in which only one of the code words in each code word pair is stored in the map.

38. The apparatus of claim **25**, in which the map pairs code words with an amount of positive word disparity with corresponding symmetric code words with the same amount of negative word disparity.

39. The apparatus of claim **25**, in which the encoder further includes a stored *m*-symbol nondata code word register, coupled to the first output of the encoder.

40. The apparatus of claim **39**, in which the *m*-symbol nondata code word is distinct from all *m*-symbol strings of consecutive symbols in all combinations of concatenated pairs of other *m*-symbol code words.

41. The apparatus of claim **39**, in which the nondata code word is distinguishable from all other code words even if a transmission error occurs in one symbol of the nondata code word.

42. The apparatus of claim **25**, each *m*-symbol code word stored by the map is selected to generally reduce susceptibility to a single-symbol error during a communication.

43. The apparatus of claim **25**, further including:

an inversion control circuit module, configured to compute a running disparity, the running disparity representing a cumulative deviation from baseline over a period of interest, the inversion control circuit module including an input coupled to the map to receive a word disparity of a code word, the inversion control circuit module configured to use the word disparity and the running disparity provide an inversion control signal at an output of the inversion control circuit module;

an inversion circuit module, including a first input coupled to the output of the inversion control circuit module to receive the inversion control signal, and including a second input coupled to the map to receive the code word, the inversion circuit module configured to invert the code word based, if indicated by the inversion control signal, and provide the resulting code word or inverted code word at a first output of the inversion module.

44. The apparatus of claim **43**, in which the inversion control signal is configured to indicate that a particular code word should be inverted if the running disparity and word disparity are both postive, and is also configured to indicate that the particular code word should be inverted if the running disparity and word disparity are both negative, and is configured to indicate that the code word should not be inverted, otherwise.

45. The apparatus of claim **25**, further including a transmitter, coupled to the first output of the encoder to receive a binary-encoded representation of the *m*-

symbol code word and to transmit a resulting pulse-amplitude-modulated multilevel signal.

46. The apparatus of claim **25**, in which the transmitter is configured to transmit the m-symbol code word using signal levels of about -100 mV, about -50 mV, about 0 V, about +50 mV, and about +100 mV.

47. A coder/decoder circuit including the apparatus of claim **25**.

48. A data communication apparatus including a decoder, the decoder including a decoder input and a decoder logic map circuit, the map circuit including a first input configured to receive a representation of an *m*-symbol code word, the map circuit configured to map the m-symbol code word to an *n*-bit block of binary data provided at a first output of the map circuit, each of the *m*-symbols in the code word including at least five possible values, each code word including:

at least one pair of adjacent symbols including a predetermined type of transition between different values of the symbols of the pair; and

a word disparity representing an cumulative deviation from a baseline of the values of the symbols of the code word, the word disparity being bounded within a predetermined range, the word disparity stored in the map corresponding to the code word.

49. The apparatus of claim **48**, in which each received *m*-symbol code word includes an intraword disparity, representing a symbol-by-symbol cumulative deviation from baseline, within the code word, and in which the intraword disparity bounded within a predetermined range.

50. The apparatus of claim **49**, in which:

each code word with a zero word disparity further includes an intraword disparity bounded within a first predetermined range;

each code word with a positive word disparity further includes an intraword disparity bounded within a second predetermined range;

each code word with a negative word disparity further includes an intraword disparity bounded within a third predetermined range; and

in which each of the first, second, and third predetermined ranges includes at least one bound that is different from at least one bound of the others of the first, second, and third predetermined ranges.

51. The apparatus of claim **50**, in which, if the five possible values are represented as (-1, -1/2, 0, +1/2, +1),

the first predetermined range is between -1.5 and +1.5, inclusive;

the second predetermined range is between -1.5 and +3.5, inclusive; and

the third predetermined range is between -3.5 and +1.5, inclusive.

52. The apparatus of claim **48**, in which each received m-symbol code word includes a word disparity bounded in a predetermined range between -2 and +2, inclusive.

53. The apparatus of claim **48**, in which the first input of the map circuit is configured to map a particular binary-encoded representation of a 6-symbol code word or pair to a particular code of a 12-bit block of binary data.

54. The apparatus of claim **48**, in which the predetermined type of transition of the m-symbol code word includes a symmetric about baseline transition.

55. The apparatus of claim **54**, in which the symmetric about baseline transition

includes a symmetric about zero transition.

56. The apparatus of claim **48**, in which each *m*-symbol code word includes:

a first bounded run length of the number of consecutive symbols, from the start of the code word, that do not include a transition of the predetermined type between adjacent ones of the symbols; and

a second bounded run length of the number of consecutive symbols, from the end of the code word, that do not include a transition of the predetermined type between adjacent ones of the symbols.

57. The apparatus of claim **56**, in which each *m*-symbol code word includes at least one of:

a first bounded run length of at least six symbols and a second bounded run length of at least five symbols; and

a first bounded run length of at least five symbols and a second bounded run length of at least six symbols.

58. The apparatus of claim **48**, in which the map decodes a pair of symmetric *m*-symbol code words with the same amount, but opposite algebraic sign, of word disparity into a unique code of the *n*-bit block of binary data.

59. The apparatus of claim **48**, in which the decoder further includes:

a comma detector circuit, coupled to the decoder input to receive a stream of multilevel symbols, and configured to detect a particular *m*-symbol nondata code word;

an *m*-symbol register, coupled to the decoder input to receive the stream of multilevel symbols, and coupled to the comma detector circuit to receive an indication of the detected particular m-symbol nondata code word, the *m*-symbol

register including an output coupled to the input of the map for providing a word-boundary-aligned *m*-symbol data code word using alignment information triggered by the detected particular *m*-symbol nondata code word.

60. The apparatus of claim **59**, in which the *m*-symbol nondata code word is distinct from all *m*-symbol strings of consecutive symbols in all combinations of concatenated pairs of other *m*-symbol code words.

61. The apparatus of claim **59**, in which the nondata code word is distinguishable from all other code words even if a transmission error occurs in one symbol of the nondata code word.

62. The apparatus of claim **48**, each *m*-symbol code mapped by the map is selected to generally reduce susceptibility to a single-symbol error during a communication.

63. The apparatus of claim **48**, in which the decoder further includes a word disparity computation circuit module, coupled to the output of the *m*-symbol register, and configured to compute, and provide at an output, the word disparity of each *m*-symbol code word provided by the *m*-symbol register to the map.

64. The apparatus of claim **63**, in which the decoder further includes a running disparity computation circuit circuit module, coupled to the output of the word disparity computation circuit module, to compute and provide at an output, a running disparity representing a cumulative deviation from baseline over a period of interest.

65. The apparatus of claim **64**, further including a disparity error checker, coupled to and using the outputs of the word disparity computation circuit module and the running disparity computation circuit module to check for a disparity error of an *m*-symbol code word provided by the *m*-symbol register to the map.

66. The apparatus of claim **65**, in which the disparity error checker includes an output indicating a disparity error, for a particular *m*-symbol code word provided by the *m*-symbol register to the map, if either: (a) the running disparity and word disparity are both positive; or (b) the running disparity and word disparity are both negative.

67. The apparatus of claim **48**, further including a receiver, including an input configured to receive a multilevel representation of an *m*-symbol code word, and including an output configured to provide a binary-encoded representation of the *m*-symbol code word.

68. The apparatus of claim **67**, in which the receiver is configured to receive the *m*-symbol code word using signal levels of about -100 mV, about -50 mV, about 0 V, about +50 mV, and about +100 mV.

69. A coder/decoder circuit including the apparatus of claim **48**.